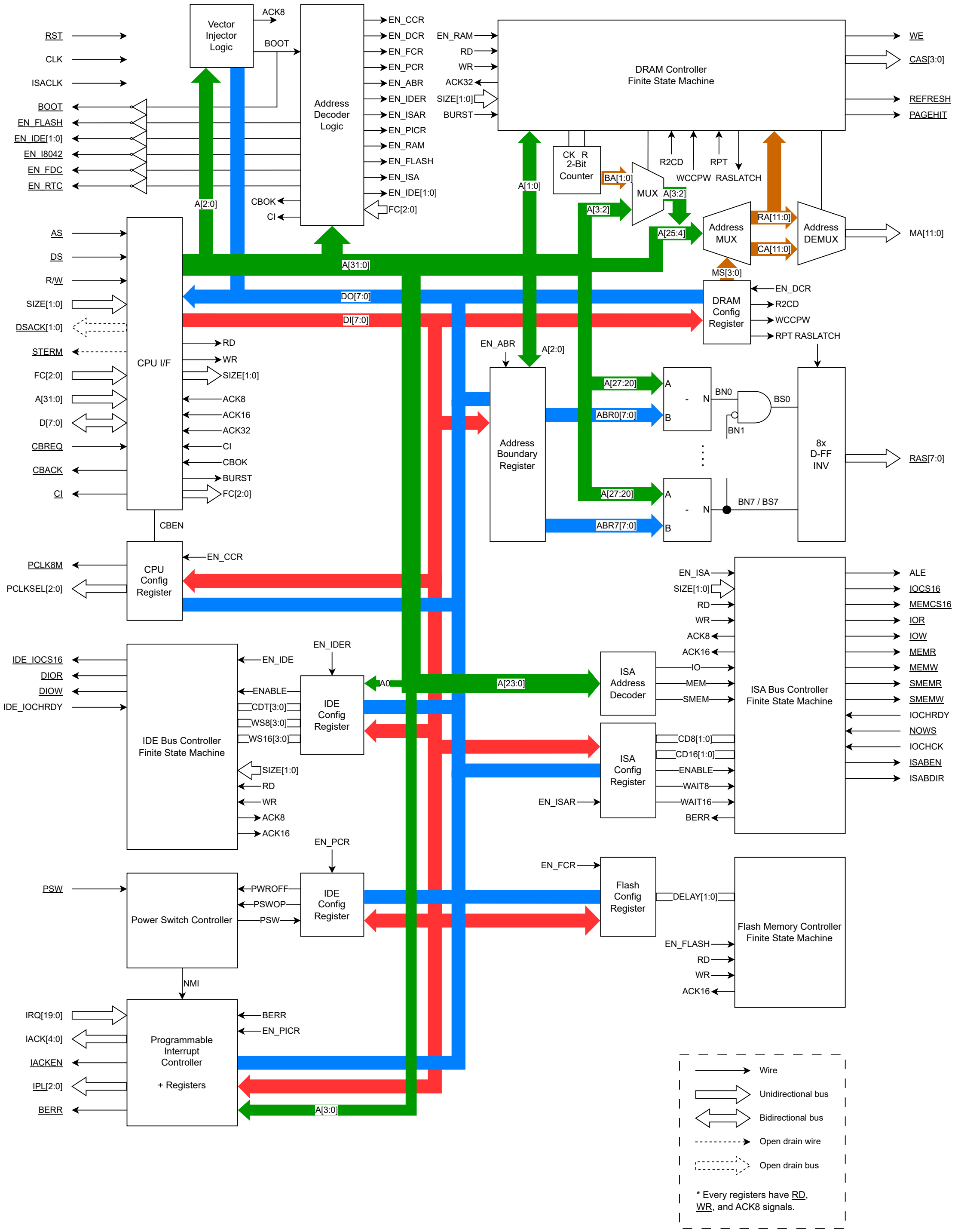
RST
CLK
ISACLK
BOOT
EN_FLASH
EN_IDE[1:0]
EN_I8042
EN_FDC
EN_RTC
Vector Injector Logic
ACK8
BOOT
Address Decoder Logic
EN_CCR
EN_DCR
EN_FCR
EN_PCR
EN_ABR
EN_IDER
EN_ISAR
EN_PICR
EN_RAM
EN_FLASH
EN_ISA
EN_IDE[1:0]
FC[2:0]
CBOK
CI
A[2:0]
EN_RAM
RD
WR
ACK32
SIZE[1:0]
BURST
DRAM Controller Finite State Machine
WE
CAS[3:0]
REFRESH
PAGEHIT
CK R 2-Bit Counter
BA[1:0]
A[1:0]
MUX
A[3:2]
R2CD
RPT
WCCPW RASLATCH
Address MUX
RA[11:0]
CA[11:0]
Address DEMUX
MA[11:0]
A[25:4]
MS[3:0]
AS
DS
R/W
SIZE[1:0]
DSACK[1:0]
STERM
FC[2:0]
A[31:0]
D[7:0]
CBREQ
CBACK
CI
CPU I/F
A[31:0]
DO[7:0]
DI[7:0]
RD
WR
SIZE[1:0]
ACK8
ACK16
ACK32
CI
CBOK
BURST
FC[2:0]
DRAM Config Register
EN_DCR
R2CD
WCCPW
RPT RASLATCH
EN_ABR
A[2:0]
Address Boundary Register
A[27:20]
ABR0[7:0]
ABR7[7:0]
A
B
N
BN0
BN1
BS0
BN7 / BS7
8x D-FF INV
RAS[7:0]
CBEN
PCLK8M
PCLKSEL[2:0]
CPU Config Register
EN_CCR
EN_ISA
SIZE[1:0]
RD
WR
ACK8
ACK16
IO
MEM
SMEM
ISA Bus Controller Finite State Machine
ALE
IOCS16
MEMCS16
IOR
IOW
MEMR
MEMW
SMEMR
SMEMW
IOCHRDY
NOWS
IOCHCK
ISABEN
ISABDIR
IDE_IOCS16
DIOR
DIOW
IDE_IOCHRDY
IDE Bus Controller Finite State Machine
EN_IDE
ENABLE
CDT[3:0]
WS8[3:0]
WS16[3:0]
SIZE[1:0]
RD
WR
ACK8
ACK16
EN_IDER
IDE Config Register
A0
A[23:0]
ISA Address Decoder
ISA Config Register
CD8[1:0]
CD16[1:0]
ENABLE
WAIT8
WAIT16
BERR
EN_ISAR
EN_PCR
PSW
Power Switch Controller
PWROFF
PSWOP
PSW
IDE Config Register
EN_FCR
Flash Config Register
DELAY[1:0]
Flash Memory Controller Finite State Machine
EN_FLASH
RD
WR
ACK16
NMI
IRQ[19:0]
IACK[4:0]
IACKEN
IPL[2:0]
BERR
Programmable Interrupt Controller
+ Registers
BERR
EN_PICR
A[3:0]
Wire
Unidirectional bus
Bidirectional bus
Open drain wire
Open drain bus
* Every registers have RD, WR, and ACK8 signals.